## Remarks/Arguments

Claims 1, 5-12, 16-23, 25 and 26 are pending in the present application. Claims 1, 12 and 23 were amended; and claims 2-4, 13-15 and 24 were canceled. No claims were added. Reconsideration is respectfully requested in view of the above amendments and the following comments.

### I. Examiner Interview

The Examiner is thanked for the courteous telephone interview granted Applicants' representative on February 27, 2007. Dependent claims 3 and 4 were discussed during the interview. In particular, Applicants' representative indicated that the portions of Hervin (U.S. Patent No. 5,805,879) referred to by the Examiner in finally rejecting claims 3 and 4 did not disclose or suggest the subject matter recited in the claims, and that the subject matter of those claims appeared to patentably distinguish over Hervin. During the interview, Applicants' representative proposed amending claim 1 to incorporate the subject matter of dependent claims 3 and 4, and to amend independent claims 12 and 23 in a similar manner in order to obtain allowance of the application.

During the interview, the Examiner acknowledged that Hervin did not appear to teach the subject matter of claims 3 and 4 in the portions of Hervin specifically referred to in the Final Office Action (column 4, lines 4-10; column 3, lines 1-3; column 2, line 62-column 3, line 7; column 3, lines 4-17). The Examiner requested, however, that Applicants' representative also review the remaining disclosure in Hervin to confirm that that Hervin did not disclose the subject matter of the claims elsewhere. This will confirm that Applicants' representative has reviewed Hervin, and believes that the subject matter that was recited in dependent claims 3 and 4, and that has now been incorporated into independent claims 1, 12 and 23, as will be discussed below, is not disclosed or suggested by Hervin.

### II. 35 U.S.C. § 101

The Examiner has rejected claims 23-26 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter.

In order to expedite prosecution, claim 23 has been amended to recite that the computer program product is in "a recordable-type computer readable medium." This terminology is supported on page 59, lines 10-12 of the specification, and clearly recites statutory subject matter that fully satisfies the requirements of 35 U.S.C. § 101.

Therefore, claims 23, 25 and 26 are directed to statutory subject matter and the rejection based on 35 U.S.C. § 101 has been overcome

## III. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-8, 10-19 and 21-26 under 35 U.S.C. § 102(b) as being anticipated by Hervin et al., U.S. Patent No. 5,805,879 (hereinafter "Hervin").

By the present Amendment, claim 1 has been amended to incorporate subject matter originally recited in dependent claims 2-4; and claims 2-4 have been canceled. In particular, claim 1 as amended herein is as follows:

> 1. A method in a data processing system for generating coverage data for accesses to dynamically allocated data during execution of code in a data processing system, the method comprising:
>
> responsive to a request to dynamically allocate a memory area for dynamically allocated data during runtime when an allocation of memory is required, dynamically allocating the memory area;
>
> responsive to dynamically allocating the memory area, associating the memory area with a data access indicator;
>
> responsive to executing an instruction in the code at a processor in the data processing system, determining whether an access to a memory location associated with the data access indicator has occurred; and
>
> if the data access indicator is associated with the memory area, changing a state of the data access indicator by the processor when the instruction is executed, wherein the coverage data for the dynamically allocated data is generated during execution of the code by the processor,
>
> wherein the memory area comprises a starting memory location and an ending memory location in which the starting memory location and the ending memory location span a size of memory equal to the request, and a subsequent memory location located one byte after the ending memory location, and wherein the data access indicator comprises a first data access indicator in a set of data access indicators associated with the memory area, wherein the first data access indicator identifies the starting memory location, and wherein the associating step further comprises:
>
> associating a second data access indicator in the set of data access indicators with the ending memory location, wherein the second data access indicator identifies the ending memory location in the memory area; and
>
> associating a third data access indicator in the set of data access indicators with the subsequent memory location, wherein the third data access indicator identifies the subsequent memory location, wherein an access to the one byte after the ending memory location indicates that a memory size of the memory area is insufficient.

As was discussed during the above-referenced interview, Hervin does not disclose or suggest a memory area that includes a starting memory location and an ending memory location in which the starting memory location and the ending memory location span a size of memory equal to the request, and a subsequent memory location located one byte after the ending memory location, and also does not disclose or suggest a data access indicator that comprises a first data access indicator in a set of data access indicators associated with the memory area that identifies the starting memory location, and does not disclose or suggest "associating a second data access indicator in the set of data access indicators with

the ending memory location, wherein the second data access indicator identifies the ending memory location in the memory area", and "associating a third data access indicator in the set of data access indicators with the subsequent memory location, wherein the third data access indicator identifies the subsequent memory location, wherein an access to the one byte after the ending memory location indicates that a memory size of the memory area is insufficient."

In rejecting the claims, the Examiner referred to column 4, lines 4-10 of Hervin as disclosing a subsequent memory location located one byte after an ending location. Column 3, line 66-Column 4, line 10 of Hervin is reproduced below for the convenience of the Examiner:

> The circuit includes: (a) exception generating circuitry to generate an exception when the segment access indicator requires setting and (b) exception handling circuitry, invoked by the processor in response to generation of the exception, to flush the execution pipeline of instructions following a segment load instruction, set the segment access indicator and load an address pointer of the processor with an address corresponding to a specified location within the segment. The "specified location within the segment" maybe the instruction following the segment load instruction or may be another instruction, as appropriate. Regardless, the processor resumes execution of instructions.

The above recitation refers to "a specified location within the segment." The recitation is not directed to a memory location located after a memory area, and is not a disclosure of a subsequent memory location located one byte after an ending location [of a memory area].

In addition, Hervin does not disclose or suggest the first, second, and third data access indicators for identifying the starting and ending locations of a size of memory, and the one byte beyond the ending location, respectively, as now recited in claim 1. The Examiner referred to column 13, lines 4-17 of Hervin, reproduced below, as disclosing the third data access indicator.

> If the access bit has not yet been set (NO branch of decisional step **715**), processor **10** generates an exception (in a step **720**), thereby effectively enabling EXI to seize or regain control of the microcode control sequences of the previous processing stages and beginning the process of setting the access bit. In response to the exception, exception-handling circuitry within the processor **10** flushes the applicable pipeline of instructions (in a step **725**) and calls a microcoded routine to handle the remainder of the exception by instructing the microsequencer of processor **10** to go, or vector, to a particular point of entry in the microROM. Those of ordinary skill in the art will recognize that the principles of present invention, although illustrated in the context of microROM instructions, may suitably be embodied in hardware or higher-level software instructions.

Applicants respectfully submit that neither the above-recitation nor anywhere else in Hervin discloses associating a "third data access indicator in a set of data access indicators with the subsequent memory location, wherein the third data access indicator identifies the subsequent memory location, wherein an access to the one byte after the ending memory location indicates that a memory size of the memory area is insufficient" as now recited in claim 1.

For at least all the above reasons, claim 1 is not anticipated by Hervin and patentably distinguishes over Hervin in its present form.

Claims 5-8, 10 and 11 depend from and further restrict claim 1, and are also not anticipated by Hervin, at least by virtue of their dependency.

Independent claims 12 and 23 have been amended in a manner similar to claim 1 and patentably distinguish over Hervin for similar reasons as discussed above with respect to claim 1. Claims 16-19, 21 and 22 depend from and further restrict claim 12, and claims 25-26 depend from and further restrict claim 23 and are also allowable in their present form, at least by virtue of their dependency.

Therefore the rejection of claims 1-8, 10-19 and 21-26 under 35 U.S.C. § 102(b) has been overcome.

## IV. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 9 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Hervin in view of Sederlund et al., U.S. Patent No. 6,647,301 (hereinafter "Sederlund"). This rejection is respectfully traversed.

Claims 9 and 20 depend from and further restrict claims 1 and 12, respectively. Sederlund does not supply the deficiencies in Hervin as described above. Accordingly, claims 9 and 20 patentably distinguish over the cited art and are allowable in their present form, at least by virtue of their dependency.

Therefore, the rejection of claims 9 and 20 under 35 U.S.C. § 103 has been overcome.

## V. Conclusion

For at least the reasons discussed above, claims 1, 5-12, 16-23, 25 and 26 patentably distinguish over the cited art and this application is believed to be in condition for allowance. It is, accordingly, respectfully requested that the Examiner enter this Amendment as placing the application in condition for allowance and issuing a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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